IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) An electronic device comprising:

a source signal line driver circuit;

a first gate signal line driver circuit;

a second gate signal line driver circuit; and

a pixel portion including a plurality of pixels,

wherein said plurality of pixels each have an EL element, an EL driving TFT for controlling luminescence of each of the EL elements, a switching TFT, and an eliminating TFT for controlling said EL driving TFT,

wherein said switching TFT is controlled by said first gate signal line driver circuit,

wherein said eliminating TFT is controlled by said second gate signal line driver circuit, and

wherein a gray-scale display is performed by controlling a luminescing time of said plurality of EL elements.

2. (Original) A device according to claim 1, wherein said switching TFT, the EL driving TFT, and the eliminating TFT are at least one of an N channel TFT or a P channel TFT.

3. (Original) A device according to claim 1, wherein said EL driving TFT becomes an OFF state when an electric potential of said power supply line is applied to said gate electrode of said EL driving TFT.

4. (Original) A computer, which uses said electronic device according to claim 1.

5. (Original) A video camera, which uses said electronic device according to claim 1.

6. (Original) A DVD player, which uses said electronic device according to claim 1.

7. (Original) An electronic device comprising:

a source signal line driver circuit connected to a plurality of source signal lines;

a first gate signal line driver circuit connected to a plurality of first gate signal lines;

a second gate signal line driver circuit connected to a plurality of second gate signal lines;

a pixel portion including a plurality of pixels; and

a power supply line,

wherein said plurality of pixels each have a switching TFT, an EL driving TFT, an eliminating TFT, and an EL element,

wherein a gate electrode of said switching TFT is connected to said first gate signal line,

wherein one of a source region and a drain region of said switching TFT is connected to said plurality of source signal lines, and another thereof is connected to a gate electrode of said EL driving TFT,

wherein a gate electrode of said eliminating TFT is connected to said second gate signal line,

wherein one of a source region and a drain region of said eliminating TFT is connected to said power supply line, and another thereof is connected to said gate electrode of said EL driving TFT, and

wherein one of a source region and a drain region of said EL driving TFT is connected to said power supply line, and another thereof is connected to said EL element.

8. (Original) A device according to claim 7, wherein said switching TFT, the EL driving TFT, and the eliminating TFT are at least one of an N channel TFT or a P channel TFT.

9. (Original) A device according to claim 7, wherein said EL driving TFT becomes an OFF state when an electric potential of said power supply line is applied to said gate electrode of said EL driving TFT.

10. (Original) A computer, which uses said electronic device according to claim 7.

11. (Original) A video camera, which uses said electronic device according to claim 7.

12. (Original) A DVD player, which uses said electronic device according to claim 7.

13. (Original) An electronic device comprising:

a source signal line driver circuit connected to a plurality of source signal lines;

a first gate signal line driver circuit connected to a plurality of first gate signal lines;

a second gate signal line driver circuit connected to a plurality of second gate signal lines;

a pixel portion including a plurality of pixels; and

a power supply line held at a constant electric potential,

wherein said plurality of pixels each have a switching TFT, an EL driving TFT, an eliminating TFT and an EL element;

wherein said EL element includes a pixel electrode, an opposing electrode held at a constant electric potential, and an EL layer formed between said pixel electrode and said opposing electrode,

wherein a gate electrode of said switching TFT is connected to said first gate signal lines,

wherein one of a source region and a drain region of said switching TFT is connected to said plurality of source signal lines, and another thereof is connected to a gate electrode of said EL driving TFT,

wherein a gate electrode of said eliminating TFT is connected to said second gate signal lines,

wherein one of a source region and a drain region of said eliminating TFT is connected to said power supply line, and another is connected to a gate electrode of said EL driving TFT, and

wherein one of a source region and a drain region of said EL driving TFT is connected to said power supply line, and another is connected to a pixel electrode of said EL element.

14. (Original) A device according to claim 13, wherein said EL layer is a low molecular organic material or a polymer organic material.

15. (Original) A device according to claim 14, wherein said low molecular organic material is made of Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

16. (Original) A device according to claim 14, wherein said polymer organic material is made of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), or polycarbonate.

17. (Original) A device according to claim 13, wherein said switching TFT, the EL driving TFT, and the eliminating TFT are at least one of an N channel TFT or a P channel TFT.

18. (Original) A device according to claim 13, wherein said EL driving TFT becomes an OFF state when an electric potential of said power supply line is applied to said gate electrode of said EL driving TFT.

19. (Original) A computer, which uses said electronic device according claim 13.

20. (Original) A video camera, which uses said electronic device according claim 13.

21. (Original) A DVD player, which uses said electronic device according to claim 13.

22. (Original) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, a pixel portion including a plurality of pixels, a plurality of source signal lines connected to said source signal line driver circuit, a plurality of first gate signal lines connected to said first gate signal line driver circuit, a plurality of

second gate signal lines connected to said second gate signal line driver circuit, and a power supply line, wherein

said plurality of pixels each have a switching TFT, an EL driving TFT, an eliminating TFT, and an EL element;

a gate electrode of said switching TFT is connected to said first gate signal lines;

one of a source region and a drain region of said switching TFT is connected to said plurality of source signal lines, and another thereof is connected to a gate electrode of said EL driving TFT;

a gate electrode of said eliminating TFT is connected to said second gate signal lines;

one of a source region and a drain region of said eliminating TFT is connected to said power supply line, and another thereof is connected a gate electrode of said EL driving TFT;

one of a source region and a drain region of said EL driving TFT is connected to said power supply line, and another thereof is connected to said EL element;

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said entire plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1);

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same; and

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$.

23. (Original) A device according to claim 22, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

24. (Original) A device according to claim 22, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

25. (Original) A device according to claim 22, wherein said switching TFT, the EL driving TFT, and the eliminating TFT are at least one of an N channel TFT or a P channel TFT.

26. (Original) A device according to claim 22, wherein said EL driving TFT becomes an OFF state when an electric potential of said power supply line is applied to said gate electrode of said EL driving TFT.

27. (Original) A computer, which uses said electronic device according to claim 22.

28. (Original) A video camera, which uses said electronic device according to claim 22.

29. (Original) A DVD player, which uses said electronic device according to claim 22.

30. (Original) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, a pixel portion including a plurality of pixels, a plurality of source signal lines connected to said source signal line driver circuit, a plurality of first gate signal lines connected to said first gate signal line driver circuit, a plurality of second gate signal lines connected to said second gate signal line driver circuit, and a power supply line held at a constant electric potential, wherein:

said plurality of pixels each have a switching TFT, an EL driving TFT, an eliminating TFT and an EL element,

said EL element includes a pixel electrode, an opposing electrode held at a constant electric potential, and an EL layer formed between said pixel electrode and said opposing electrode;

a gate electrode of said switching TFT is connected to said first gate signal lines;

one of a source region and a drain region of said switching TFT is connected to said plurality of source signal lines, another thereof is connected to a gate electrode of said EL driving TFT;

a gate electrode of said eliminating TFT is connected to said second gate signal lines,

one of a source region and a drain region of said eliminating TFT is connected to said power supply line, and another thereof is connected to a gate electrode of said EL driving TFT;

one of a source region and a drain region of said EL driving TFT is connected to said power supply line, and another thereof is connected to a pixel electrode of said EL element;

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1),

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same; and

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$.

31. (Original) A device according to claim 30, wherein said EL layer is a low molecular organic material or a polymer organic material.

32. (Original) A device according to claim 30, wherein said low molecular organic material is made of Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

33. (Original) A device according to claim 30, wherein said polymer organic material is made of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), or polycarbonate.

34. (Original) A device according to claim 30, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

35. (Original) A device according to claim 30, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

36. (Original) A device according to claim 30, wherein said switching TFT, the EL driving TFT, and the eliminating TFT are at least one of an N channel TFT or a P channel TFT.

37. (Original) A device according to claim 30, wherein said EL driving TFT becomes an OFF state when an electric potential of said power supply line is applied to said gate electrode of said EL driving TFT.

38. (Currently Amended) A computer, which uses said electronic device according to ~~any one of claims 1 through 19~~ claim 30.

39. (Original) A video camera, which uses said electronic device according to claim 30.

40. (Original) A DVD player, which uses said electronic device according to claim 30.

41. (Original) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, a pixel portion including a plurality of pixels, a plurality of source signal lines connected to said source signal line driver circuit, a plurality of first gate signal lines connected to said first gate signal line driver circuit, a plurality of second gate signal lines connected to said second gate signal line driver circuit, and a power supply line, wherein:

said plurality of pixels each have a switching TFT, an EL driving TFT, an eliminating TFT, and an EL element;

a gate electrode of said switching TFT is connected to said first gate signal lines;

one of a source region and a drain region of said switching TFT is connected to said plurality of source signal lines, and another thereof is connected to a gate electrode of said EL driving TFT;

a gate electrode of said eliminating TFT is connected to said second gate signal lines;

one of a source region and a drain region of said eliminating TFT is connected to said power supply line, and another thereof is connected a gate electrode of said EL driving TFT;

one of a source region and a drain region of said EL driving TFT is connected to said power supply line, and another thereof is connected to said EL element

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period,;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said entire plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1);

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same;

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$, and

said display periods Tr1, Tr2, ···, Tr(n) appear in a random order.

42. (Original) A device according to claim 41, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

43. (Original) A device according to claim 41, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

44. (Original) A device according to claim 41, wherein said switching TFT, the EL driving TFT, and the eliminating TFT are at least one of an N channel TFT or a P channel TFT.

45. (Original) A device according to claim 41, wherein said EL driving TFT becomes an OFF state when an electric potential of said power supply line is applied to said gate electrode of said EL driving TFT.

46. (Original) A computer, which uses said electronic device according to claim 41.

47. (Original) A video camera, which uses said electronic device according to claim 41.

48. (Original) A DVD player, which uses said electronic device according to claim 41.

49. (Original) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, a pixel portion including a plurality of pixels, a plurality of source signal lines connected to said source signal line driver circuit, a

plurality of first gate signal lines connected to said first gate signal line driver circuit, a plurality of second gate signal lines connected to said second gate signal line driver circuit, and a power supply line held at a constant electric potential, wherein:

said plurality of pixels each have a switching TFT, an EL driving TFT, an eliminating TFT and an EL element;,

said EL element includes a pixel electrode, an opposing electrode held at a constant electric potential, and an EL layer formed between said pixel electrode and opposing electrode;

a gate electrode of said switching TFT is connected to said first gate signal lines;

one of a source region and a drain region of said switching TFT is connected to said plurality of source signal lines, and another thereof is connected to a gate electrode of said EL driving TFT;

a gate electrode of said eliminating TFT is connected to said second gate signal lines;

one of a source region and a drain region of said eliminating TFT is connected to said power supply line, and another thereof is connected a gate electrode of said EL driving TFT;

a source region and a drain region of said EL driving TFT, wherein one is connected to said power supply line whereas the other is connected to a pixel electrode of said EL element;

an (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and an (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) (m is an arbitrary integer from 2 to (n)) are provided in 1 frame period;

digital data signals from said source signal line driver circuit are fed to all said plurality of pixels through said plurality of source signal lines in said writing-in periods Ta1, Ta2, ···, Ta(n);

the digital data signals fed to said plurality of pixels are all eliminated in said eliminating periods Te1, Te2, ···, Te(m-1);

among said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n), a portion of the writing-in periods Ta1, Ta2, ···, Ta(m) and a portion of said eliminating periods Te1, Te2, ···, Te(m-1) overlap with each other;

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m-1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) are display periods Tr1, Tr2, ···, Tr(m-1);

periods from the start of each of said eliminating periods Te1, Te2, ···, Te(m-1) to the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are non-display periods Td1, Td2, ···, Td(m-1);

periods from the start of each of the writing-in periods Ta1, Ta2, ···, Ta(m+1) in said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) to the start of the next writing-in periods of each of said writing-in periods Ta(m), Ta(m+1), ···, Ta(n), respectively, are display periods Tr(m), Tr(m+1), ···, Tr(n);

in said display periods Tr1, Tr2, ···, Tr(n), said plurality of EL elements are selected by said digital data signals to luminesce or not luminesce;

a length of said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) and a length of said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are the same;

ratios of the lengths of said display periods Tr1, Tr2, ···, Tr(n) are expressed as 2^0: 2^1: ···: $2^{(n-1)}$; and

said display periods Tr1, Tr2, ···, Tr(n) appear in a random order.

50. (Original) A device according to claim 49, wherein said EL layer is a low molecular organic material or a polymer organic material.

51. (Original) A device according to claim 49, wherein said low molecular organic material is made of Alq_3 (tris-8-quinolilite-aluminum) or TPD (triphenylamine derivative).

52. (Original) A device according to claim 49, wherein said polymer organic material is made of PPV (polyphenylene vinylene), PVK (polyvinyl carbazole), or polycarbonate.

53. (Original) A device according to claim 49, wherein said (n) number of writing-in periods Ta1, Ta2, ···, Ta(n) are not overlapped with each other.

54. (Original) A device according to claim 49, wherein said (m-1) number of eliminating periods Te1, Te2, ···, Te(m-1) are not overlapped with each other.

55. (Original) A device according to claim 49, wherein said switching TFT, the EL driving TFT, and the eliminating TFT are at least one of an N channel TFT or a P channel TFT.

56. (Original) A device according to claim 49, wherein said EL driving TFT becomes an OFF state when an electric potential of said power supply line is applied to said gate electrode of said EL driving TFT.

57. (Original) A computer, which uses said electronic device according to claim 49.

58. (Original) A video camera, which uses said electronic device according to claim 49.

59. (Original) A DVD player, which uses said electronic device according to claim 49.

60. (Original) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion including a plurality of pixels,

wherein said plurality of pixels have a plurality of EL elements, and

wherein respective drives of said plurality of EL elements are controlled by a digital data signal outputted from said source signal line driver circuit, a first selecting signal outputted from said first gate signal line driver circuit, and a second selecting signal outputted from said second gate signal line driver circuit.

61. (Original) A computer, which uses said electronic device according to claim 60.

62. (Original) A video camera, which uses said electronic device according to claim 60.

63. (Original) A DVD player, which uses said electronic device according to claim 60.

64. (Original) An electronic device comprising a source signal line driver circuit, a first gate signal line driver circuit, a second gate signal line driver circuit, and a pixel portion including a plurality of pixels,

wherein said plurality of pixels includes a plurality of EL elements; and

wherein a luminescing time of said EL element is controlled by a digital data signal outputted from said source signal line driver circuit, a first selecting signal outputted from said first gate signal line driver circuit, and a second selecting signal outputted from said second gate signal line driver circuit, to thereby perform gray-scale display.

65. (Original) A computer, which uses said electronic device according to claim 64.

66. (Original) A video camera, which uses said electronic device according to claim 64.

67. (Original) A DVD player, which uses said electronic device according to claim 64.